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10/532,848	04/27/2005	**Bert Braune**	12406-112US1 P2002,0914 U	1921

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EXAMINER	
YANG, MINCHUL	
ART UNIT	**PAPER NUMBER**
2891	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/532,848	BRAUNE ET AL.	
	Examiner	Art Unit	
	MINCHUL YANG	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/27/05,3/11/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A broad range or limitation together with a narrow range or limitation that falls within the broad range or limitation (in the same claim) is considered indefinite, since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. See MPEP § 2173.05(c). Note the explanation given by the Board of Patent Appeals and Interferences in Ex parte Wu, 10 USPQ2d 2031, 2033 (Bd. Pat. App. & Inter. 1989), as to where broad language is followed by "such as" and then narrow language. The Board stated that this can render a claim indefinite by raising a question or doubt as to whether the feature introduced by such language is (a) merely exemplary of the remainder of the claim, and therefore not required, or (b) a required feature of the claims. Note also, for example, the decisions of Ex parte Steigewald, 131 USPQ 74 (Bd. App. 1961); Ex parte Hall, 83 USPQ 38 (Bd. App. 1948); and Ex parte Hasche, 86 USPQ 481 (Bd. App. 1949). In the present instance, claim 1 recites the broad recitation "an LED light source" and the narrow recitation "particularly comprising mixed-color LEDs". For the remainder of this Office action, only the broad recitation is considered on the merits. Any claim not specifically addressed above is being rejected as incorporating the deficiencies of a claim

upon which it depends. Appropriate correction is required.

3. Claim 2-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites a limitation "said luminescence conversion material comprises a radioparent matrix material that is replaced with a phosphor". This limitation is inconsistent with the description in the specification (page 2, line 23), "The luminescence conversion element ordinarily comprises a phosphor embedded in a matrix material". Moreover, the specification does not disclose how to replace a radioparent matrix material with a phosphor. For further examination, it is assumed that this limitation is intended to mean "said luminescence conversion material comprises a radioparent matrix material and a phosphor material" and has been treated as such for the remainder of this Office action. Any claim not specifically addressed above is being rejected as incorporating the deficiencies of a claim upon which it depends. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-8 and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Tatsunori (JP Pub. 2002118293: previously made of record of IDS).

Tatsunori discloses a method for producing an LED light source, particularly comprising mixed-color LEDs, wherein at least a portion of primary radiation emitted by a chip is transformed by luminescence conversion, comprising the steps of (see, e.g., figures 3a-e and related text):

Regarding claim(s) 1: preparing a chip (2) comprising a front-side electrical contact (5) in the form of an electrical contact surface, thickening said front-side electrical contact by applying an electrically conductive material (8) to said electrical contact surface, coating said chip with a luminescence conversion material (9);

Regarding claim(s) 2-4: wherein said luminescence conversion material comprises a radioparent matrix material that is replaced with a phosphor (paragraph 0042: the $(Y, Gd)_3(Al, Ga)_5O_{12}$:Ce wavelength conversion material comprises radioparent matrix material Al_2O_3 as a host matrix material and (Y, Gd) as a phosphor); wherein said radioparent matrix material comprises SiO_2 and/or Al_2O_3; wherein said radioparent matrix material comprises an oxide and/or a nitride whose refractive index is between 1.5 and 3.4 (Al_2O_3 has a refractive index between 1.5 and 3.4);

Regarding claim(s) 5-6, 8: wherein electrical terminals (8) that are coated with luminescence conversion material (9) are then exposed by thinning the luminescence conversion material (see, e.g., figure 3c); wherein the layer of luminescence conversion material is evened by thinning (see, e.g., figure 3c); wherein the thickness of the layer of luminescence conversion material is adjusted by thinning it (see, e.g., figure 3c);

Regarding claim(s) 7: wherein monitoring of the color coordinates (CIE chromaticity diagram) of the LED light source is subsequently performed (0070);

Regarding claim(s) 10: wherein the chip emitting the primary radiation is disposed in a wafer composite with a multiplicity of additional similar chips (see, e.g., 0012), each of the method steps takes place simultaneously for the chips of the entire wafer composite (see figures 3a-d and related text), the chips are subsequently singulated into LED light sources (figure 3e);

Regarding claim(s) 11: wherein before the chips are coated with luminescence conversion material, troughs (figure 3a: the troughs between the adjacent LED chips) are made along scribe lines between the individual chips, so that during the subsequent coating of the chips with luminescence conversion material said troughs are at least partially filled with luminescence conversion material (figure 3b).

6. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Maeda (US Pub. 2002/0028527).

Maeda discloses a method for producing an LED light source, particularly comprising mixed-color LEDs, wherein at least a portion of primary radiation emitted by a chip is transformed by luminescence conversion, comprising the steps of (see, e.g., figures 5 and 13a-c; and related text):

Regarding claim(s) 1: preparing a chip (5 in figure 10a) comprising a front-side electrical contact (17 and 18 in figure 5) in the form of an electrical contact surface, thickening said front-side electrical contact by applying an electrically conductive material (25) to said electrical contact surface, coating said chip with a luminescence conversion material (3: see also 0105);

Regarding claim(s) 2-4: wherein said luminescence conversion material comprises a radioparent matrix material that is replaced with a phosphor (0106: the $(Y, Gd)_3(Al, Ga)_5O_{12}$:Ce wavelength conversion material comprises radioparent matrix material Al_2O_3 as a host matrix

material and (Y, Gd) as a phosphor); wherein said radioparent matrix material comprises SiO_2 and/or Al_2O_3; wherein said radioparent matrix material comprises an oxide and/or a nitride whose refractive index is between 1.5 and 3.4 (Al_2O_3 has a refractive index between 1.5 and 3.4);

Regarding claim(s) 6: wherein the layer of luminescence conversion material is evened by thinning (see, e.g., figure 13b and related text);

Regarding claim(s) 7: wherein monitoring of the color coordinates (CIE chromaticity diagram) of the LED light source is subsequently performed (0105);

Regarding claim(s) 8: wherein the thickness of the layer of luminescence conversion material is adjusted by thinning it (0109-0112 and figure 13b: polishing is performed to adjust the thicknesses of the luminescence conversion material 3).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c)

and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda, as applied to the claims above, and further in view of Inoue (US Pub. 2002/0081773).

Maeda discloses the features outlined above, and further discloses that the color coordinates of the LED device is adjusted by controlling the thickness of the layers of luminescence conversion (0105 and 0109-0112) using a thinning method. Maeda does not expressly teach that the coordinates of the LED device are monitored during thinning. However, it was common in the art that monitoring optical characteristics of LED devices was performed at a wafer-level before dicing the wafer. For instance, Inoue teaches a method of monitoring optical characteristics of LED devices at a wafer-level before dicing the wafer (see, e.g., figures 35 and 0295). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the Maeda teachings with the Inoue teachings to thin the luminescence conversion layer during being monitored. One would have been motivated to do so in order to reduce manufacturing time and cost.

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tatsunori, as applied to the claims above, and further in view of Kumar (US Pub. 2003/0077878).

(a) Tatsunori discloses the features outlined above, but does not expressly teach the following limitations: wherein before the chips are coated with luminescence conversion material, the entire wafer composite is mounted with the underside on a carrier, the chips are singulated from the wafer composite in such a way that they continue to be held together on said carrier, during the coating of the chips, the lateral sides of the singulated chips are at least partially coated with luminescence conversion material, the chips are subsequently singulated

into LED light sources from their composite held together by said carrier and said luminescence conversion material.

However, Kumar teaches a method of singulating a semiconductor chip using a wafer carrier (see, e.g., figure 3d and related text), wherein an entire wafer composite (100) is mounted with the underside on a carrier (300), the chips are singulated from the wafer composite in such a way that they continue to be held together on said carrier (figure 3d), the chips are subsequently singulated from their composite held together by said carrier. Kumar teaches that this method can benefit to avoid the chipping and cracking problems caused by conventional dicing methods (0005-0006). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the Kumar method of singulating chips in the method of Tatsunori in order to avoid the chipping and cracking problems caused by conventional dicing methods. It would also have been obvious to one of ordinary skill in the art at the time of the invention to perform the coating step after the step of singulating the wafer on the wafer carrier in order to simplify the wafer singulating step without need to singulate the coating.

11. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tatsunori, as applied to the claims above, and further in view of Inoue.

Tatsunori discloses the features previously outlined, but does not expressly teach the following limitation(s): wherein before said chips are singulated into LED light sources their respective color coordinates and positions are determined and recorded, and after singulation the LED light sources are sorted on the basis of their color coordinates.

However, it was common in the art that monitoring optical characteristics of LED devices was performed at a wafer-level before being singulated. For instance, Inoue teaches a method of

monitoring optical characteristics of LED devices at a wafer-level before being singulated (see, e.g., figures 35 and 0295). It was also common in the art that the step of monitoring optical characteristics of LED devices at a wafer-level included recording positions and color coordinates. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the Tatsunori teachings with the Inoue teachings to determine and record color coordinates and positions of the LED devices before being singulated in order to reduce manufacturing time and cost. It would also have been obvious to one of ordinary skill in the art at the time of the invention to sort the singulated LED devices on the basis of their color coordinates, because color of emitting light from the device was critical for applications such as a white light source and a light source for a memory disc.

12. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tatsunori, as applied to the claims above, and further in view of Inoue and Maeda.

Tatsunori in view of Inoue teach the following limitation(s), as addressed above regarding claim 13: before the chips are singulated, determining and recording the respective color coordinates and positions of the LED light sources, and monitoring the color coordinates of one of the LED light sources of the region concerned.

Tatsunori in view of Inoue do not expressly teach the following limitation(s): dividing the wafer into regions containing LED light sources that have similar color coordinates, adjusting the regions containing LED light sources that have similar color coordinates to a specific set of color coordinates by regionally selective thinning of the luminescence conversion material in the individual regions. However, Maeda discloses that the color coordinates of the LED device is adjusted by controlling the thickness of the layers of luminescence conversion (0105 and 0109-

0112) using a thinning method. Maeda further discloses that each LED device can be selectively thinned in order to adjust its color coordinates (0109-0110 and figures 7a-b). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to perform a selective thinning for a pre-determined region in the wafer of Tatsunori, as taught by Inoue and Maeda, in order to optimize color coordinates such that the color coordinates of the regions are the same or different from each other. The examiner also notes that where the general conditions of a claim are disclosed in prior art, provision for adjustability where needed involves only routine skill in the art.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minchul Yang whose telephone number is (571) 270-1750. The examiner can normally be reached on Monday through Friday 7:30 AM - 5:00 PM E.S.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272 -1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MY /M. Y./

Examiner, Art Unit 2891

/Matthew C. Landau/

Primary Examiner, Art Unit 2815